What is claimed is:

1. A decoding method of a Viterbi decoder, the Viterbi decoder having a branch metric unit, an add-compare-select unit and a path memory unit, the method comprising the steps of:

performing a longitudinal arrangement with respect to a trellis diagram corresponding to the Viterbi decoder so as to obtain a longitudinal arrangement trellis diagram;

processing the longitudinal arrangement trellis diagram according to a run length limited (RLL) code so as to obtain a RLL trellis diagram;

computing a current input branch-metric value by the branch metric unit according to the RLL trellis diagram;

obtaining a next state value by computing the current input branch-metric value, a next input branch-metric value and a current state by the add-compare-select unit so as to obtain a next state value;

recording results computed by the add-compare-select unit in the path memory unit so as to obtain a survivor path; and

decoding the recorded survivor path.

2. The decoding method according to claim 1, further comprising the step of creating the trellis diagram corresponding to the Viterbi decoder before the step of performing the longitudinal arrangement.

3. The decoding method according to claim 2, wherein the step of performing the longitudinal arrangement is performed several times.

4. The decoding method according to claim 3, wherein the step of obtaining a next state value sets a current output decision bit and a next output decision bit according to only the next state value.

5. The decoding method according to claim 4, wherein the branch metric value

computed according to the RLL trellis diagram is inputted into the add-compare-select unit so as to become one of the current input branch-metric value and the next input branch-metric value.

6. The decoding method according to claim 5, wherein the method for recording the survivor path in the path memory unit is one of a shuffle-exchange method and a trace-back method.

7. The decoding method according to claim 6, wherein a set of memory is provided for each state of the trellis diagram corresponding to the Viterbi decoder in the shuffle-exchange method so as to record the survivor path reaching the state value.

8. The decoding method according to claim 6, wherein the trace-back method comprises the steps of:

recording a decision bit of a previous state value and the current state value according to the current output decision bit and the next output decision bit;

comparing the relationship between the current state value and the decision bit;

writing the decision bit into the suitable state value;

writing an extension bit, which is the same as a first bit of the state value, into the state when the state of the decision bit is not recorded;

outputting the decision bit to a trace write-in register array and tracing for obtaining a merged value, wherein the decoding register array becomes an idling register array when the decision bit stored in a decoding register array reaches a predetermined amount; and

decoding the decision bit stored in the previous idling register array according to the merged value.

9. A decoding method of a Viterbi decoder, the Viterbi decoder having a branch

metric unit, an add-compare-select unit and a path memory unit having a decoding register array, a trace write-in register array and an idling register array, the method comprising the steps of:

creating a original trellis diagram corresponding to the Viterbi decoder;

performing a longitudinal arrangement with respect to the original trellis diagram so as to obtain a longitudinal arrangement trellis diagram;

processing the longitudinal arrangement trellis diagram according to a RLL code so as to obtain a RLL trellis diagram;

computing a branch metric value by the branch metric unit according to the RLL trellis diagram;

computing a current input branch-metric value, a next input branch-metric value and a current state by the add-compare-select unit so as to obtain a next state value;

setting a current output decision bit and a next output decision bit by the add-compare-select unit according to only the next state value;

recording a decision bit on a previous state value and the current state value according to the current output decision bit and the next output decision bit;

comparing a relationship between the current state value and the decision bit;

writing the decision bit into the suitable state value;

outputting the decision bit from the add-compare-select unit to the trace write-in register array and tracing for obtaining a merged value, wherein the decoding register array becomes the idling register array when the decision bit stored in the decoding register array reaches a predetermined amount; and

decoding the decision bit stored in the previous idling register array according

to the merged value.

10. The decoding method according to claim 9, wherein the step of performing the longitudinal arrangement with respect to the original trellis diagram is performed several times.

11. The decoding method according to claim 10, wherein the branch metric value computed according to the RLL trellis diagram is inputted into the add-compare-select unit so as to become one of the current input branch-metric-value and the next input branch-metric-value.

12. A decoding circuit of a Viterbi decoder, the decoding circuit comprising a branch metric unit, an add-compare-select unit and a path memory unit, the branch metric unit computing a branch metric value and outputting the branch metric value to the add-compare-select unit, the add-compare-select unit computing an optimum path of a state value according to the branch metric value and outputting a decision bit, the path memory unit comprising:

a data string controller for receiving the decision bit outputted from the add-compare-select unit and deciding the direction of the output string of the decision bit;

a trace write-in register array for receiving the decision bit outputted from the data string controller and tracing to obtain a merged value;

an idling register array for storing the merged value obtained from the tracing of the trace write-in register array; and

a decoding register array for decoding the decision bit stored in the decoding register array according to the merged value obtained by the tracing.

13. The decoding circuit according to claim 12, wherein the decoding register array becomes the idling register array when the decision bit stored in the decoding register array reaches a predetermined amount.

14. The decoding circuit according to claim 13, wherein when the trace write-in register array traces and obtains the merged value and provides the merged value to the idling register array, the idling register array becomes the decoding register array and decodes acccording to the merged value.

15. The decoding circuit according to claim 14, further comprising, between the trace write-in register array and the idling register array:

a first state retrieve circuit performing bidirectional data transmission with the trace write-in register array and capable of outputting data;

a first delay register for receiving the data outputted from the first state retrieve circuit, delaying a period of time, and then outputting the data; and

a second state retrieve circuit for receiving the data outputted from the first delay register and perfomring bidirectional data transmission with the idling register array.

16. The decoding circuit according to claim 15, further comprising, between the trace write-in register array and the decoding register array:

a third state retrieve circuit performing bidirectional data transmission with the trace write-in register array and capable of outputting data;

a second delay register for receiving the data outputted from the third state retrieve circuit, delaying a period of time, and then outputting the data; and

a fourth state retrieve circuit for receiving the data sent by the second delay register, and performing bidirectional data transmission with the decoding register array.

17. The decoding circuit according to claim 16, wherein data access is performed between the first state retrieve circuit and a memory block and a state register of the register array, and the first state retrieve circuit further comprises:

a first decision circuit having a plurality of decision signal input terminals for receiving output data from the state register, and having a selection signal output terminal for outputting a selection signal;

a first multiplexer having a plurality of input terminals for receiving data of the memory block, a selection terminal for receiving data of the state register, and an output terminal for outputting data; and

a second multiplexer having input terminals for receiving output data from the state register and the output terminal of the first multiplexer, a selection terminal for receiving the selection signal outputted from the selection signal output terminal of the first decision circuit, and a output terminal for outputting data to the state register.

18. The decoding circuit according to claim 16, wherein data access is performed between the second state retrieve circuit and the memory block and the state register of the register array, and the second state retrieve circuit further comprises:

a second decision circuit having the plurality of decision signal input terminals for receiving output data from the state register, and having the selection signal output terminal for outputting the selection signal;

a third multiplexer having a plurality of input terminals for receiving data of the memory block, a selection terminal for receiving data of the state register, and a output terminal for outputting data; and

a fourth multiplexer having input terminals for receiving output data from the state register and the output terminal of the third multiplexer, a selection terminal for receiving the selection signal outputted from the selection signal output terminal of the second decision circuit, and a output terminal for outputting data to the state register.

19. The decoding circuit according to claim 16, wherein data access is performed between the third state retrieve circuit and the memory block and the state register of the register array, and the third state retrieve circuit further comprises:

a third decision circuit having a plurality of decide signal input terminals for receiving output data from the state register, and having the selection signal output terminal for outputting the selection signal;

a fifth multiplexer having a plurality of input terminals for receiving data of the memory block, a selection terminal for receiving data of the state register, and a output terminal for outputting data; and

a sixth multiplexer having input terminals for receiving output data from the state register and the output terminal of the fifth multiplexer, a selection terminal for receiving the selection signal outputted from the selection signal output terminal of the third decision circuit, and a output terminal for outputting data to the state register.

20. The decoding circuit according to claim 16, wherein data access is performed between the fourth state retrieve circuit and the memory block and the state register of the register array, and the fourth state retrieve circuit further comprises:

a fourth decision circuit having a plurality of decide signal input terminals for receiving output data from the state register, and having the selection signal output terminal for outputting the selection signal;

a seventh multiplexer having the plurality of input terminals for receiving data of the memory block, the selection terminal for receiving data of the state register, and a output terminal for outputting data; and

an eighth multiplexer having input terminals for receiving output data from the

state register and the output terminal of the seventh multiplexer, the selection terminal for receiving a selection signal outputted from the selection signal output terminal of the fourth decision circuit, and a output terminal for outputting data to the state register.